

Form PTO 1449 (Rev. 2-32)		U.S. Department of Commerce Patent and Trademark Office		JUN 07 2004		Atty. Docket No. IMPJ-0004		Serial No. 10/681,577	
Information Disclosure Statement by Applicant						Applicant: Christopher J. Diorio et al.		Filed: October 7, 2003	
(Use several sheets if necessary)						Group: 2816			
U.S. Patent Documents									
Init.		Document No.	Date	Name	Class	Subclass	Filing Date		
HN	A	4,783,783	11/08/1988	Nagai et al.	365	202	277		
	B	4,935,702	06/19/1990	Mead et al.	365	202	277		
	C	5,933,039	08/03/1999	Hui et al.	365	202	277		
	D	5,939,945	08/17/1999	Thewes et al.	365	202	277		
	E	6,134,182	10/17/2000	Pilo et al.	365	202	277		
	F	6,320,788	11/20/2001	Sansbury et al.	365	202	277		
Foreign Documents									
Init.		Document No.	Date	Country	Class	Subclass	Translation		
HN	G	0 298 618 A	01/11/1989	EP					
Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)									
HN	H	Partial International Search for International Application No. PCT/US03/31792, date mailed April 2, 2004.							
HN	I	Carley, L. Richard, "Trimming Analog Circuits Using Floating-Gate Analog MOS Memory", IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1569-1575, December 1989.							
Examiner					Date Considered				
HAI L. NOUYER					12/02/04				
Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.									

